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NOTICE OF ALLOWANCE AND FEE(S) DUE

000181 7590 08/12/2003

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MCLEAN, VA 22102-3833

EXAMINER	
SCHILLINGER, LAURA M	
ART UNIT	CLASS-SUBCLASS
2813	438-257000

DATE MAILED: 08/12/2003

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/987,884	11/16/2001	Yoshihiro Ikeda	XA-9582	7583

TITLE OF INVENTION: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND MANUFACTURING METHOD THEREOF

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1300	$300	$1600	11/12/2003

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED A ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

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B. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

If the SMALL ENTITY is shown as NO:

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B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclo the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.

☐ Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

[redacted]RT B - FEE(S) TRANSMITTAL [redacted]

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed wh appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" maintenance fee notifications.

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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with t United States Postal Service with sufficient postage for first class mail in envelope addressed to the Box Issue Fee address above, or being facsimi transmitted to the USPTO, on the date indicated below.

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EXAMINER	ART UNIT	CLASS-SUBCLASS
SCHILLINGER, LAURA M	2813	438-257000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment h been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) ❑ individual ❑ corporation or other private group entity ❑ governm

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❑ Publication Fee
❑ Advance Order - # of Copies _____

4b. Payment of Fee(s):

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(Authorized Signature) (Date)

NOTE; The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Alexandria, Virginia 22313-1450.

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EXAMINER	
SCHILLINGER, LAURA M	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 08/12/2003

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The patent term adjustment to date is 0 days. If the issue fee is paid on the date that is three months after the maili date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) af the mailing date of this notice, the term adjustment will be 0 days.

If a continued prosecution application (CPA) was filed in the above-identified application, the filing date th determines patent term adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retriev (PAIR) system. (http://pair.uspto.gov)

Any questions regarding the patent term extension or adjustment determination should be directed to the Office Patent Legal Administration at (703)305-1383.

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UNITED STATES

DATE MAILED: 08/12/2003

Notice of Fee Increase on January 1, 2003

If a reply to a "Notice of Allowance and Fee(s) Due" is filed in the Office on or after January 1, 2003, then the amount due will be higher than that set forth in the "Notice of Allowance and Fee(s) Due" since there will be an increase in fees effective on January 1, 2003. See Revision of Patent and Trademark Fees for Fiscal Year 2003; Final Rule, 67 Fed. Reg. 70847, 70849 (November 27, 2002).

The current fee schedule is accessible from: http://www.uspto.gov/main/howtofees.htm.

If the issue fee paid is the amount shown on the "Notice of Allowance and Fee(s) Due," but not the correct amount in view of the fee increase, a "Notice to Pay Balance of Issue Fee" will be mailed to applicant. In order to avoid processing delays associated with mailing of a "Notice to Pay Balance of Issue Fee," if the response to the Notice of Allowance and Fee(s) due form is to be filed on or after January 1, 2003 (or mailed with a certificate of mailing on or after January 1, 2003), the issue fee paid should be the fee that is required at the time the fee is paid. If the issue fee was previously paid, and the response to the "Notice of Allowance and Fee(s) Due" includes a request to apply a previously-paid issue fee to the issue fee now due, then the difference between the issue fee amount at the time the response is filed and the previously paid issue fee should be paid. See Manual of Patent Examining Procedure, Section 1308.01 (Eighth Edition, August 2001).

Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL-85 (REV. 05-03) Approved for use through 04/30/2004.

Notice of Allowability	Application No.	Applicant(s)	
	09/987,884	IKEDA ET AL.	
	Examiner	Art Unit	
	Laura M Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *5/29/03*.
2. ☒ The allowed claim(s) is/are *11-32*.
3. ☒ The drawings filed on *16 November 2001* are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. ☐ CORRECTED DRAWINGS must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No. ____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☐ Notice of References Cited (PTO-892)
3☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
5☐ Information Disclosure Statements (PTO-1449), Paper No. ____.
7☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
2☐ Notice of Informal Patent Application (PTO-152)
4☐ Interview Summary (PTO-413), Paper No.____ .
6☐ Examiner's Amendment/Comment
8☒ Examiner's Statement of Reasons for Allowance
9☐ Other

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

This Office Action is in response to Amendment B, dated 5/29/03, in Paper No.8.

Allowable Subject Matter

Claims 11-32 are allowed.

The following is an examiner's statement of reasons for allowance:

In reference to claim 11, Hashimoto teaches a method for manufacturing a semiconductor IC including a MIS transistor structure comprising:

a) forming a first gate insulating film for forming the MIS transistor structure on a main surface of the semiconductor substrate (Fig.25b (31));

b) forming at least one pair of laminating structure bodies each including two layers of a first gate electrode (32 and 39) covering a part of the first gate insulating film (31) and a first insulating film covering the first gate electrode (41), an etching prevention film being formed on a sidewall portion of the first insulating film(Col.10, lines: 25-27-see also Col.6, lines: 55-60);

c) introducing impurities into the semiconductor substrate through the first gate insulating film located in a region uncovered with the laminating structure bodies, and thereby forming a first impurity introduced region self-aligned with the laminating structure bodies on the main surface of the semiconductor substrate (Col.9, lines: 50-60 and Fig.22(a) and see also Fig.s 23 and 26 a) (38));

d) removing the first gate insulating film in the region uncovered with the laminating structure bodies after step (c) (Fig.26a- uncovered regions are not 31 (gate insulating layer but rather are FOX regions 30); and

e) forming a second insulating film covering upper portions and sidewall portions of the laminating structure bodies after step (d) (Fig.26 a and Col.10, lines: 25-27- 41 is an oxide-nitride-oxide film).

In reference to claim 19, Hashimoto teaches a method comprising the steps of:

a) forming on a main surface of a semiconductor substrate, a first gate insulating film consisting of a SiO film (31), a second gate insulating film (51) and a second conductive film (55A) over the first gate insulating film in this order (Fig. 36 –2(a));

b) forming a first protection insulating film consisting of one of a single layer film (Fig.39a (54, 42)) and a laminating film, the single layer film being a SiO film formed over the second conductive film (Col.12, lines: 30-35), and the laminating film being a SiN film formed over the SiO film Col.12, lines: 50-55);

c) patterning the first protection insulating film and thereby forming an etching mask consisting of the first protection insulating film;

d) patterning the second conductive film the second gate insulating film and the first conductive film in this order by dry etching using the etching mask as a mask (Col.11, lines: 50-55 and Col.12, lines: 35-40), and thereby forming a plurality of gate electrodes that each have a floating gate electrode (50) consisting of the first conductive filmCol.11, lines: 50-65) and a control gate electrode (55A) consisting of the second conductive film (52 and 53) and that each have a laminating structure in which an upper portion of the gate electrode is covered with the first protection insulating film (54, 42).

e) forming a etching prevention film consisting of a SiN film on both sidewall portion of the first protection insulating film patterned, after step (c) and before the step (d) or after step (d) (Col.12, liens: 50-55);

f) introducing impurities into the main surface of the semiconductor substrate located between sidewall portions facing each other in the plurality of gate electrodes, and thereby forming source and drain regions (Col.12, lines: 45-55);

g) treating a surface of the semiconductor substrate by using etchant containing HF acid after step (F) and thereby cleaning the first gate insulating film located between the sidewall portions which face each other in the plurality of gate insulating film (Col.6, lines: 5-10).

h) covering an upper portion of both sidewall portions of the gate electrode (50) and forming a second protection insulating film consisting of a SiN film having such a thickness as to partially embed a region between the sidewall portions which face each other in the plurality of gate electrodes (Fig.37 (a) (51));

i) forming on an upper portion of the second protection insulating film, an interlayer insulating film consisting of SiO and embedding with the interlayer insulating film, the region between the sidewall portions which face each other in the plurality of gate electrodes (Fig.37 (a) (51)- 51 is an ONO film and therefore includes both an N and O layer);

j) etching the interlayer insulating film and second protection insulating film located between the sidewall portions which face each other in the plurality of gate electrodes (51), and thereby forming a first connection hole (Fig.39 (56))for exposing a surface of the source region and a second connection hole for exposing a surface of the drain region (56); and

k) forming a third conductive film electrically connected to the source region inside the first connection hole (Fig.43 (a) (58)), and forming a fourth conductive film electrically connected to the drain inside the second conductive hole (Fig.43(a) (64)).

However, as Applicant pointed out in his arguments dated 6/5/03, Hashimoto fails to teach nor suggest Applicant's amended claim limitation that the etching prevention film being formed on a sidewall portion of the first insulating film **but so as not to cover sidewall portions of the first gate electrode (floating gate/control gate).** Rather, Hashimoto teaches forming the film to cover the sidewall portions (See Fig.39 (55)). Applicant argues that his patterned etch prevention film allows for removal of damaged gate oxide films without reducing the width of the gate (See Amendment A, page 15, first paragraph, lines 8-11). The Examiner considers such an argument persuasive. Further, Hashimoto makes no suggestion to modify his teachings to include such a step. Consequently, claims 1-32 are deemed allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (703) 308-6425. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LMS
August 7, 2003